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(54) Digital signal processing apparatus and method

(57) The invention provides for signal processing apparatus (100) having a first filter means (102) for adjusting an input signal based on past data output from the apparatus (130), a summing means (106) is arranged to sum signals from the first filter means (102) and from a second filter means (104) to produce a sum signal. The apparatus also includes a symbol detection means (108) for generating an output signal from the sum signal and the second filter means (104) is arranged to provide adjustments in the output signal based on the peaks and polarity of past signals generated by the symbol detection means (108). A control means can be included for controlling the filtering properties of both the first and second filter means, wherein the control means controls the filtering properties based on the past output signals from the symbol detection means.

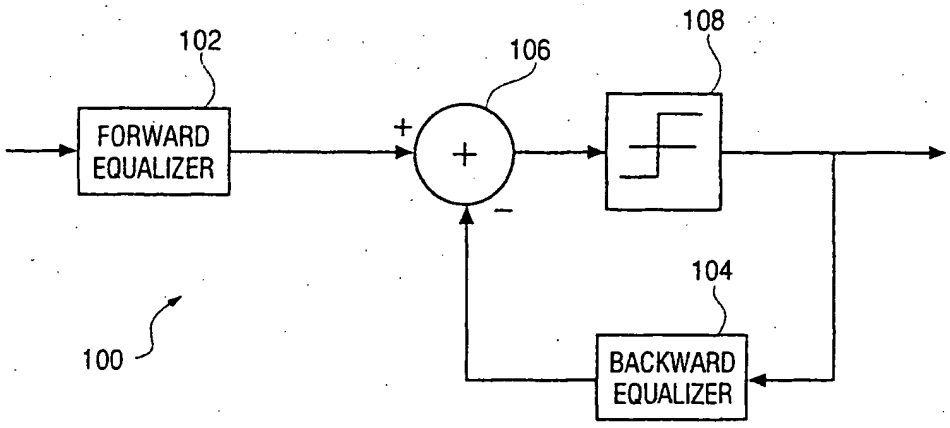

FIG. 1

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Description

The present invention provides for a digital signal processing apparatus and method, and in particular, but not exclusively, to an improved decision feedback equalizer for digital signal transmissions.

The advent of the information age has increased the demand for the storage of digital data, along with the demands for processing and transmission of such data. The density of information stored in a single system has been increased to accommodate the growing demand. For example, the capacity of magnetic disks storage units has grown fuelled by improvements in the design of heads and disks, improvements in magnetic media, decreases in head gap length and flying height, and improvements in servo accuracy for increased track density.

The growing demand for digital storage capacity has also prompted an interest in the use of digital signal processing methods as a means of continuing increases in density. The general similarity of read and write processes in disk and tape drive units to data detection in transmission and communication systems has focussed interest on the application of equalization and coding methods to channels for both tape and disk drive systems. In particular, read channels have received special attention because the information has to be processed faster. Equalizers are used in both tape and disk drive read channels. In particular, decision feedback equalizers have been used to recover digital signals in read channels. Two types of noise dominate magnetic recording and read channels. One is regular noise caused by thermal noise in electronics and random variations in the magnetic media. The other type of noise is intersymbol interference (ISI). Regular noise is found everywhere and effects all channels. ISI becomes worse with increasing density. Pulses generated by transitions in the magnetic media tend to overlap as transitions become closer with higher recording densities. Many of these decision feedback equalizers incorporate finite impulse response (FIR) filters to reduce errors caused by interference between successive pulses of data. This interference is also known as intersymbol interference (ISI). Additionally, errors may occur when the peaks of positive and negative pulses do not have the same magnitude.

Presently available equalizers used in read channels contain coefficients that are determined to reduce errors in data transmission (e.g., ISI). The presently available adaptive equalizers adapt or alter coefficients based on an error signal derived from errors in the output of the read channel. These equalizer coefficients, however, are not optimal for all possible types of data patterns. Therefore, it would be advantageous to have an improved apparatus for equalizing signals to reduce errors in transmission of data.

According to one aspect of the present invention there is provided digital signal processing apparatus comprising first filter means for adjusting an input signal, summing means for summing signals from the first filter means and from second filter means to produce a summed signal, symbol detection means for generating an output signal from the summed signal, wherein the second filter means is arranged for adjusting the output signal; and the apparatus further comprises control means for controlling the first filter means and the second filter means based on past output signals from the symbol detection means.

Preferably the first filter means can comprise a filter bank containing a plurality of filters, wherein one of the plurality of filters is selected by the control means for filtering the input signal.

Advantageously, the symbol detection means comprises a slicer and, further, the first filter means can comprise a first filter and the second filter means can comprise a second filter, wherein the filtering properties of the first filter and the second filter can be adapted in response to past data patterns passing through the signal processing apparatus.

Further, the data patterns produced in the output signal preferably comprise the polarity of the output signals.

The apparatus can advantageously be provided in the form of a decision feedback equalizer for processing data signals and which can therefore comprise a first finite impulse response filter unit having an input and an output, wherein data signals are received at the input, a summing circuit having a first input, a second input, and an output, the first input being connected to the output of the first finite impulse response filter unit, a symbol detector having an input and an output, the input being connected to the output of the summing circuit, wherein the output of the symbol detector produces digital data, a second finite impulse response filter unit having an input and an output, wherein the input of the second finite impulse response filter unit is connected to the output of the symbol detector and the output of the second finite impulse response filter unit is connected to the second input of the summing circuit and a selection logic unit having a connection to the first finite impulse response filter unit and the second finite impulse response filter unit, wherein the selection logic unit controls the first finite impulse response filter unit and the second finite impulse response filter based on output digital data from the symbol detector.

Preferably the first finite impulse response filter unit is arranged to sharpen the leading edge of data signals received at the input and the second finite impulse response filter unit is arranged to cancel tails after positive and negative pulses in the data signals.

Advantageously, the first finite impulse response filter unit includes a finite impulse response filter having an input for a set of coefficients and a memory connected to the finite impulse response filter when the memory contains a number of sets of coefficients used in response to different data patterns transmitted through the

decision feedback equalizer.

Preferably, the different data patterns comprise pulse polarities.

Advantageously, the apparatus can be arranged such that the past data includes different patterns of logic ones and logic zeros.

Advantageously, the second finite impulse response filter unit comprises a finite impulse response filter having an input for a set of coefficients and a memory connected to the finite impulse response filter, wherein the memory includes a number of sets of coefficients generated in response to past data transmitted through the decision feedback equalizer.

The first finite impulse response filter unit can advantageously comprise a plurality of finite impulse response filters.

According to another aspect of the present invention there is provided a method of adjusting a filter in a digital signal processing apparatus comprising transmitting a plurality of different data patterns through the apparatus wherein the plurality of different data patterns are filtered by the filter, producing a set of coefficients for the filter in response to each of the plurality of different data patterns to produce a number of sets of coefficients, selecting a set of coefficients within the number of sets of coefficients based on a previous data pattern generated by the apparatus and utilizing the selected set of coefficients to filter data travelling through the apparatus.

Also, the present invention can provide for a magnetic data storage system comprising a read head for reading data from a magnetic disk in the disk drive system, a preamplifier unit connected to the read head, a read channel including an antialiasing unit having an input and an output, wherein the input is connected to the preamplifier unit, an analog to digital converter having an input and an output, wherein the input is connected to the output of the antialiasing filter and a decision feedback equalizer comprising apparatus as defined above.

The invention can therefore advantageously provide for signal processing apparatus having a first filter means for adjusting an input singal based on past data output from the apparatus. In addition, a summing means can be used to sum signals from the first filter means and from a second filter means to produce a summed signal. The apparatus may also include a symbol detection means for generating an output signal from the summed signal and the second filter means can be arranged to provide adjustments in the output signal based on the peaks and polarity of past signal generated by the symbol detection means. Further, a control means can be included for controlling the filtering properties of both the first and second filter means, wherein the control means controls the filtering properties based on the past output signals from the symbol detection means.

The above as well as additional objectives, features, and advantages of the present invention will become apparent in the following detailed description.

The invention is described further hereinafter, by way of example only, with reference to the accompanying drawings in which:

Fig. 1 is a block diagram of a decision feedback equalizer (DFE) depicted in accordance with an embodiment of the present invention;

Figs. 2A-2D are more detailed block diagrams ofDFEs depicted in accordance with an embodiment of the present invention;

Fig. 3 is a flowchart of a process for calculating FIR filter coefficients based on data patterns and peak magnitudes of pulses depicted according to an embodiment of the present invention;

Fig. 4 is a block diagram of a read channel depicted according to an embodiment of the present invention; and

Figs. 5A and 5B are disk drive systems depicted in which DFEs may be implemented into read channels, such as read channel 500 in Fig. 4 according to an embodiment of the present invention.

With reference now to the figures, and in particular with reference to Fig. 1, a block diagram of a decision feedback equalizer (DFE) 100 is depicted in accordance with a preferred embodiment of the present invention. DFE 100 includes a forward equalizer 102, a backward equalizer 104, a summing circuit 106, and a symbol detector 108, such as, for example, a slicer. DFE 100 is used for suppressing inter-symbol interference (ISI) in high density magnetic recording, according to the present invention. Forward equalizer 102 receives an analog input waveform according to the present invention. Forward equalizer 102 filters the signal based on prior data patterns in accordance with a preferred embodiment of the present invention. The filtered signal is sent to summing circuit 106, which sums the signal from forward equalizer 102 and from backward equalizer 104 to produce a summed signal. Backward equalizer 104 modifies the signal by subtracting the trailing edges of pulses in the waveform in accordance with a preferred embodiment of the present invention. The trailing edges of a positive pulse and a negative pulse can be different. Slicer 108 produces a best estimate of the data symbol, given an input from summing circuit 106.

According to the present invention, DFE 100 sets the coefficients in forward equalizer 102 based on the data pattern generated by symbol detector 108 rather than on an error measure as is the case for presently available adaptive equalizers. Similarly, the coefficients in backward equalizer 104 are selected on the basis of the polarity of past pulses rather than on a measurement of error in the output from DFE 100 according to the present invention. These coefficients are selected to reduce errors caused by various data patterns and peaks having different magnitudes.

For example, forward equalizer 102 in DFE 100 can

be designed to compensate for various effects in the magnetic read channel. Forward equalizer 102 is employed to sharpen the leading edge of pulses received by DFE 100. Under linear channel assumptions, without noise, a single set of forward equalizer coefficients is optimal for all data patterns. According to a preferred embodiment of the present invention, forward equalizer 102 has coefficients adapted for filtering pulses based on the polarity of the waveform as determined by symbol detector 108. Typically with MR heads, a bigger pulse occurs in one direction than the other. Forward equalizer 102 is adapted to correct for the difference between the pulse sizes. While forward equalizer 102 does not know what bit is coming next, the expected polarity of the next pulse can be determined from the output of symbol detector 108. With magnetic media, the polarity of the next pulse is opposite of the last pulse. For example, if a "0" comes next, nothing will be present to equalize but if a "1" is next, forward equalizer 102 can be set correctly for the polarity for the pulse using different sets of coefficients according to the present invention. Once noise, however, is added potential problems can arise in that some data patterns are more susceptible to noise than other data patterns. Thus, designing or setting forward equalizer 102 with less noise boost for the most noise sensitive patterns usually reduces this type of susceptibility and improves performance within the read channel.

Alternatively, forward equalizer 102 also can be set based on past data patterns in the form of a series of zeros and ones. For example, if the most error prone pattern were an isolated one, such as 0 0 0 1 0 0 0, the three zeros could be detected and the coefficients switched from the normal forward equalizer coefficients, optimized over all patterns, to a second set of coefficients that is optimized for patterns with three leading zeros. Forward equalizer 102 adjusts for past data patterns. Backward equalizer 104 is used to adjust for offsets between peaks in a signal.

Backward equalizer 104 subtracts off the trailing edges of pulses. Similarly, the coefficients in backward equalizer 104 could be altered depending on the polarity of the pulses and the magnitude of the peaks of the pulses according to the present invention. According to the present invention, forward equalizer 102 and backward equalizer 104 may be implemented either by using an adaptive or time varying filter and placing different sets of coefficients within the equalizers depending on the past data. Alternatively, forward equalizer 102 and backward equalizer 104 may be implemented using a number of different filters, with each filter having a fixed set of coefficients according to the present invention. In particular, the coefficients for the filters are identified using a time domain adaptive filter method called least means square (LMS), which uses a training sequence and adjusts the filter coefficients to obtain the right response. More information of DFEs may be found in Proakis, *Digital Communications,* McGraw-Hill, Inc., 3d ed., 1995, ISBN No. 0-07-051726-6. More information on filters, filter design, and selection of coefficients for filters may be found in Ifeachor and Jervis, *Digital Signal Processing: A Practical Approach,* Addison-Wesley Publishers Company, Inc., 1995, ISBN No. 0-201-54413-X. More information of the use of DFEs with respect to magnetic recording can be found in Cioffi, et al., *Adaptive Equalization in Magnetic-Disk Storage Channels,* IEEE Communications Magazine, February 1990, pages 14-29 and *Density Improvements in Digital Magnetic Recording by Decision Feedback Equalization,* Bergmans, IEEE transactions on Magnetics, vol. MAG-22, number 3, May 1986, pages 157-162. According to a preferred embodiment of the present invention, LMS is preferred for determining filter coefficients.

With reference now to Figs. 2A-2D, more detailed block diagrams of DFEs are depicted in accordance with a preferred embodiment of the present invention. According to the present invention the forward equalizers (e.g., a filter bank containing FIR filters or a single FIR filter connected to a memory containing different sets of coefficients) are employed to sharpen the leading edges of pulses based on a data pattern, such as a series of logic zeros followed by a logic one or on the expected polarity of the next pulse. The backward equalizer cancels tails based on the polarity of the pulses according to the present invention. The backward equalizer detects the polarity of the pulse and knows that the trailing edge will interfere with the next pulse and the proper set of coefficients is selected to cancel the trailing edge to eliminate interference according to the present invention. DFE 300 in Fig. 2A includes a filter bank 302 containing FIR filters 304, 306, and 308 according to the present invention. The outputs of FIR filters 304, 306, and 308 in filter bank 302 are connected to summing circuit 304 with the output of summing circuit 304 being connected to slicer 306. DFE 300 also includes a backward equalizer 308 with the output bits from slicer 306 used as an input into backward equalizer 308 as in a conventional DFE. Additionally, the data bits from slicer 306 are directed into selection logic 310, which selects one of FIR filters 304, 306, or 308 in filter bank 302 based on the data output from slicer 306 according to the present invention. In this manner, the best FIR filter in filter bank 302 may be selected for a given prior data pattern for different symbol decisions generated by slicer 308 to minimize data errors caused by a particular data pattern according to the present invention.

Although filter bank 302 contains FIR filters, other filters may be implemented in accordance with a preferred embodiment of the present invention. For example, infinite impulse response (IIR) filters or continuous time filters may be implemented in place of FIR filters 304, 306, and 308. Although the depicted example shows only three filters, other numbers of filters may be implemented according to the present invention.

In Fig. 2B, DFE 312 employs a single FIR filter 314 with time varying coefficients instead of a filter bank 302

in Fig. 3A. Different sets of coefficients are stored within coefficient memory 316. A set of coefficients from the different sets of coefficients is selected from coefficient memory 316 by selection logic 310 in response to data patterns output by slicer 306 according to the present invention. The set of coefficients selected for use in FIR filter 314 is selected to minimize data errors caused by a particular waveform being sent through DFE 312 according to the present invention.

Slicer 306 should be able to provide immediate decisions on each symbol so that selection logic 310 can function properly. Although the depicted examples show a slicer, such as slicer 306, more complex detectors can be employed according to the present invention. For example, slicer 306 maybe employed to estimate pulse polarity and a more complex detector may be employed to generate feedback bits according to the present invention.

Feedback cancellation terms for cancelling ISI caused by positive and negative pulses having different peak magnitudes may be implemented within an FIR filter 318 in DFE 320 in Fig. 2C as coefficients according to the present invention. Different sets of coefficients are used to provide feedback cancellation terms, depending on the polarity and magnitude of the pulse whose ISI is being cancelled. These coefficients are stored within coefficient memory 322 and are designed to cancel tails caused by a positive and a negative pulse having different peak magnitudes according to the present invention. The particular sets of coefficients used by FIR filter 318 are selected by selection logic 310 based on the output from slicer 306.

Alternatively, the FIR filter 318 may be implemented in DFE 324 in Fig. 2D using a filter bank 326 according to the present invention. Filter bank 326 includes FIR filter 328 and FIR filter 330, which have their outputs connected to summing circuit 304. The output of slicer 306 is routed to FIR filter 328 or FIR filter 330, based on pulse polarity, using separator 332. If the output of slicer 306 is being directed to FIR filter 328, a zero is being directed to FIR filter 330, and vice versa. FIR filter 328 and FIR filter 330 each contain coefficients that result in positive and negative pulses cancelling to eliminate the occurrence of tails. In this manner, the presently claimed invention reduces data errors.

With reference now to Fig. 3, a flowchart of a process or calculating FIR filter coefficients based on patterns or polarities of pulses is depicted according to the present invention. The LMS algorithm is used in each case, and two or more sets of FIR filter coefficients are calculated at once. A long sequence of pulses, called a training sequence, is used in the LMS algorithm. A known data sequence, which represents the correct binary pattern for the training sequence is also used in the LMS algorithm.

In Fig. 3, coefficients of all filters are initialized in step 400. Next, training data is fed into each filter, (step 402) and all filter outputs are calculated (step 404). The filter outputs are compared to the known data sequence, generating an error signal for each FIR filter (step 406). A determination is made as to whether the error signal is less than a preselected limit or value (step 408). If the error is small enough, the process is terminated. If not, the FIR filter coefficients are adapted to reduce the error (step 410). Note that coefficients for each FIR filter are only adapted at those points in the training sequence where that filter will be used. In this way, the LMS algorithm is used to train several filters at once. Following step 410, the process is repeated starting at step 402 until the error is reduced to an acceptable level. Many variations of this process are possible, based on known methods in adaptive filtering. The coefficients determined in this process are then stored in coefficient memories 316 and 322 for use in the respective FIRs or they are used to generate FIRs for use in filter banks according to the present invention. More information on calculating FIR filter coefficients using LMS may be found in Ifeachor and Jervis, *Digital Signal Processing: A Practical Approach,* Addison-Wesley Publishers Company, Inc., 1995, ISBN No. 0-201-54413-X.

With reference now to Fig. 4, a block diagram of a read channel is depicted according to the present invention. Read channel 500 includes automatic gain control 502, which receives an input signal from a read head (not shown). The adjusted signal is sent to antialiasing filter 504 for initial modification and then to analog to digital (A/D) converter 506. Thereafter, the signal is modified by DFE 508 in the manner described above.

With reference now to Figs. 5A and 5B, magnetic data storage systems, a disk drive system 600 and a tape drive system 602, are depicted in which DFEs may be implemented into read channels, such as read channel 500 in Fig. 4 according to the present invention.

Nonlinear effects are common in magnetic recording, and these can be partially compensated by forward equalizer 102 according to the present invention. Magneto resistive (MR) heads have several nonlinear characteristics that give rise to asymmetric dipulses. By keeping track of the pulse polarity, the selection logic can easily switch between two backward equalizers or two sets of coefficients one for positive pulses and one for negative pulses.

Manufacturing variation is one cause of MR head nonlinearities. Thus, a disk drive with several MR heads may contain several different types of nonlinearity. In such a situation, several sets of FIR filter coefficients can be used and chosen based on prior data and on the particular MR head being used. The coefficients may be determined through a training sequence performed during manufacturing or on power up to generate the filter coefficients for use with each individual MR head. Additionally, different coefficients may be used for each head in a multi-head drive system.

Thus, the present invention provides an improved method and apparatus for filtering data by employing a DFE having a forward equalizer whose filtering proper-

ties can be varied in response to past data output by the apparatus (e.g., a series of zeros and a one or pulse polarity). Additionally, the present invention provides additional processing of data signals using a backward equalizer that has filtering properties that can be varied in response to peaks of positive and negative pulses already processed by the apparatus.

The forward equalizer contains coefficients varying with time, being chosen from a set of possible coefficients. The selection logic examines past data and loads the best set of filter coefficients at each symbol time. Thus, the forward equalizer is tuned to specific data patterns or pulse polarity for optimal performance. Similarly, the backward equalizer has its coefficients selected based on the polarity of the detected data. The use of specific data patterns and polarity of detected data provides for optimal performance when the apparatus of the present invention is used in read channels for drive systems, such as disk drive system 600 and tape drive system 602. Thus, with the present inventions nonlinear characteristics caused by MR heads and by various read channels may be minimized using a DFE according to the present invention.

While the invention has been particularly shown and described with reference to preferred embodiments, it will be understood by those skilled in the art that the invention is not restricted to the foregoing embodiments. For example, although the present invention is described with the respect to the magnetic recording channels, such as recording channels in a tape drive system or a disk drive system, the equalizers of the present invention maybe employed in other types of data channels.

Claims

1. Digital signal processing apparatus (100) comprising:

   first filter means (102) for adjusting an input signal;
   summing means (106) for summing signals from the first filter means (102) and from second filter means (104) to produce a summed signal;
   symbol detection means (108) for generating an output signal from the summed signal;
   wherein the second filter means (104) is arranged for adjusting the output signal; and
   the apparatus further comprises control means (310) for controlling the first filter means (102) and the second filter means (104) based on past output signals from the symbol detection means (108).

2. Apparatus as claimed in Claim 1, wherein the control means (310) is arranged to control the filtering properties of the first filter means (102) based on data patterns produced in the output signal and is arranged to control the filtering properties of the second filter means (104) based on the polarity of output signals generated by the symbol detection means (108).

3. Apparatus as claimed in Claim 1, wherein the first filter means comprises a finite impulse response filter (314).

4. Apparatus as claimed in Claim 3, wherein the finite impulse response filter (314) is a time varying finite impulse response filter having an input for a set of coefficients, and the apparatus further comprises a memory (316) connected to the finite impulse response filter (314), the memory (316) containing a number of sets of coefficients produced in response to a plurality of different data patterns generated by the symbol detection means (108, 306).

5. Apparatus as claimed in Claim 4, wherein the memory (316) is connected to the finite impulse response filter by the control (310) means, and the control means (310) includes a connection to the symbol detection means (306) and is arranged to select a set of coefficients from the number of coefficients based on data in the output signal already generated by the symbol detection means (306).

6. Apparatus as claimed in Claim 5, wherein the second filter means (104) comprises a second finite impulse response filter (318) having an input for a set of coefficients, and the apparatus further comprises a second memory (322) connected to the second finite impulse response filter (318), the memory containing a second number of sets of coefficients produced in response to a plurality of different data patterns generated by the symbol detection means, wherein the second memory (322) is connected to the second finite impulse response filter (318) by control means (310), which is arranged to include a connection to the symbol determination means (306) and selects a set of coefficients from the second number of coefficients based on data in the output signal already generated by the symbol determination means (306).

7. Apparatus as claimed in any one of Claims 1-6, and arranged as a decision feedback equalizer for processing data signals.

8. A method for adjusting a filter in a digital signal processing apparatus comprising:

   transmitting a plurality of different data patterns through the apparatus wherein the plurality of different data patterns are filtered by the filter;

producing a set of coefficients for the filter in response to each of the plurality of different data patterns to produce a number of sets of coefficients;
selecting a set of coefficients within the number of sets of coefficients based on a previous data pattern generated by the apparatus; and
utilizing the selected set of coefficients to filter data traveling through the apparatus.

9. A magnetic data storage system comprising:

read head for reading data from a magnetic disk in the disk drive system;
a preamplifier unit connected to the read head;
a read channel (500) including:

an antialiasing unit (504) having an input and an output, wherein the input is connected to the preamplifier unit;
an analog to digital converter (506) having an input and an output, wherein the input is connected to the output of the antialiasing filter (504); and
a decision feedback equalizer (508) comprising apparatus as claimed in any one of Claims 1-6.

10. A magnetic data storage system as claimed in Claim 9 and further comprising an automatic gain control unit (502) having an input and an output, wherein the input of the antialiasing unit (504) is connected to the preamplifier by the automatic gain control unit (502) and the input of the automatic gain control unit (502) is connected to the preamplifier unit.

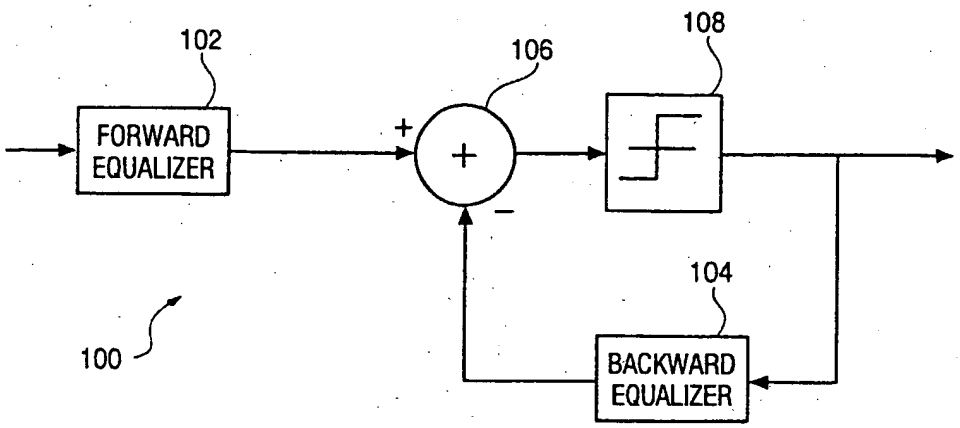
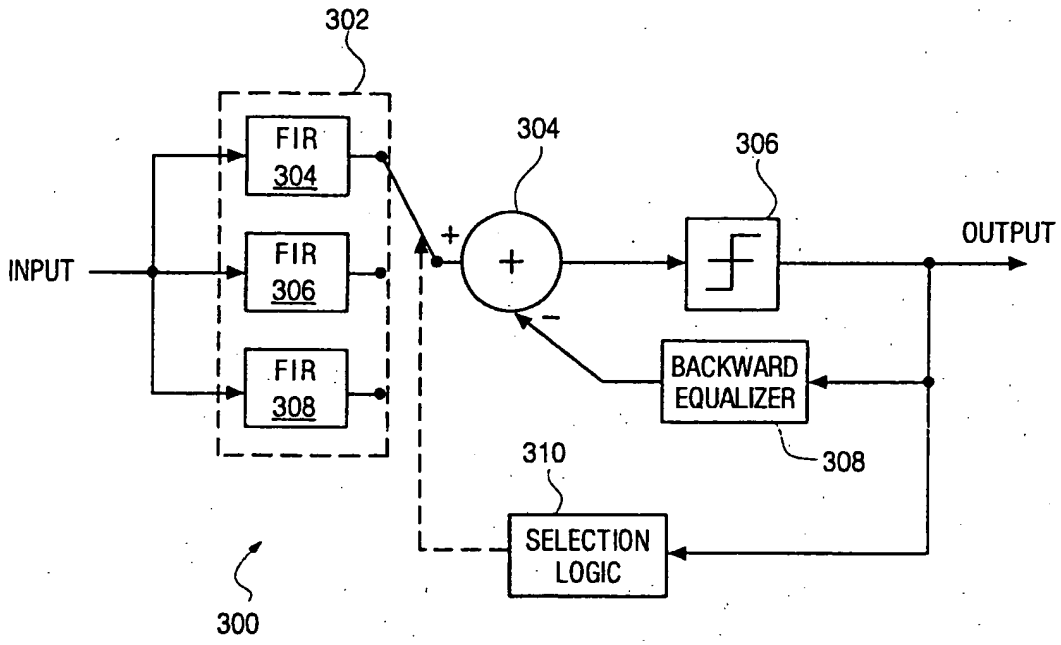


FIG. 1


302
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304
FIR
306
FIR
308
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306
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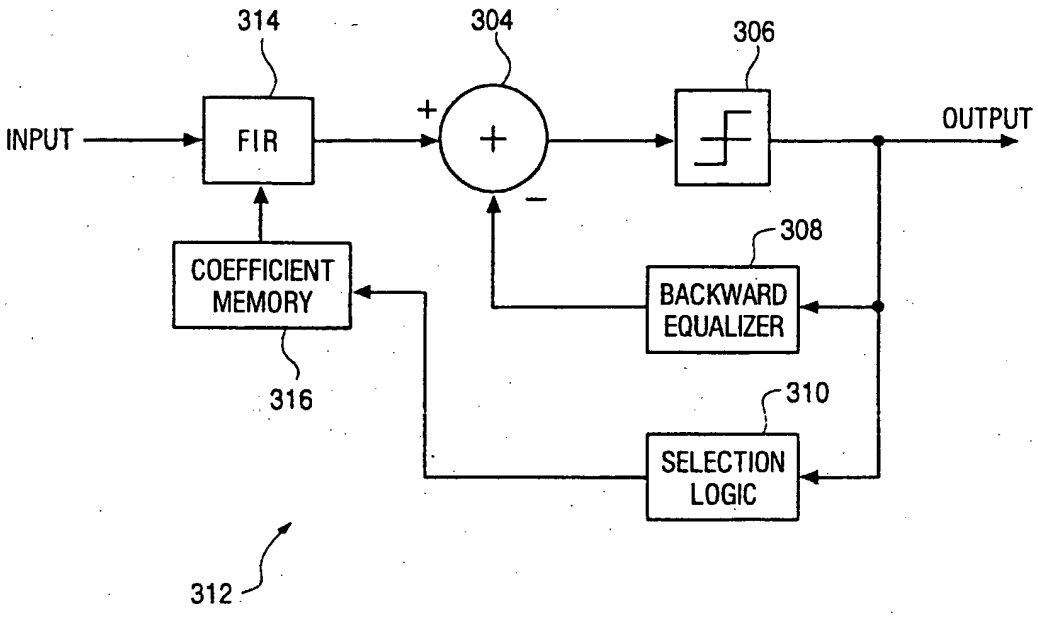
+
−
OUTPUT
BACKWARD
EQUALIZER
308
310
SELECTION
LOGIC
300

FIG. 2A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306
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FIR
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+
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OUTPUT
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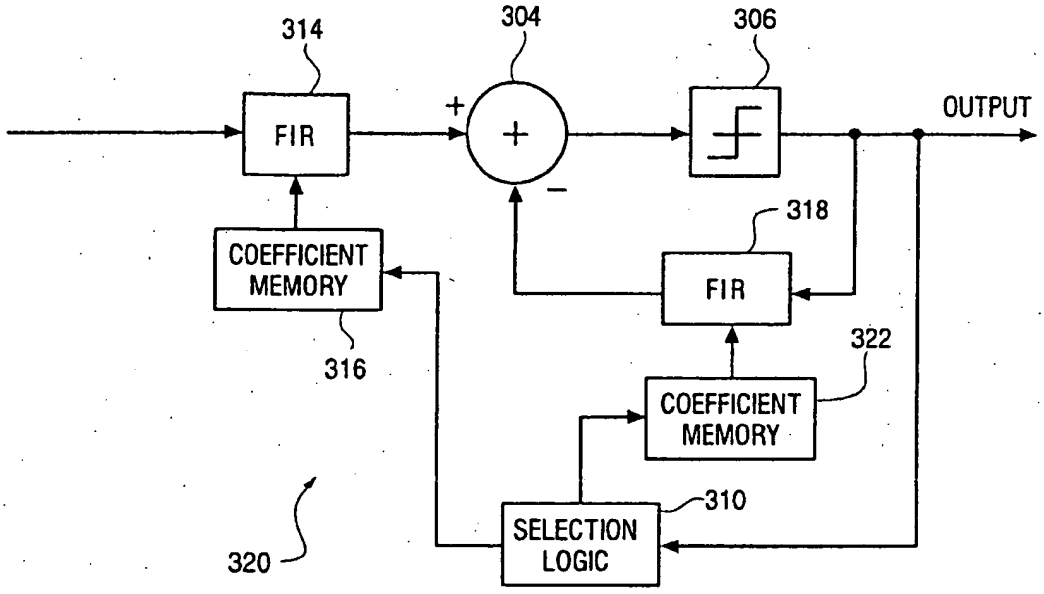
COEFFICIENT MEMORY
BACKWARD EQUALIZER
316
310
SELECTION LOGIC
312

FIG. 2B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306
FIR
+
+
−
OUTPUT
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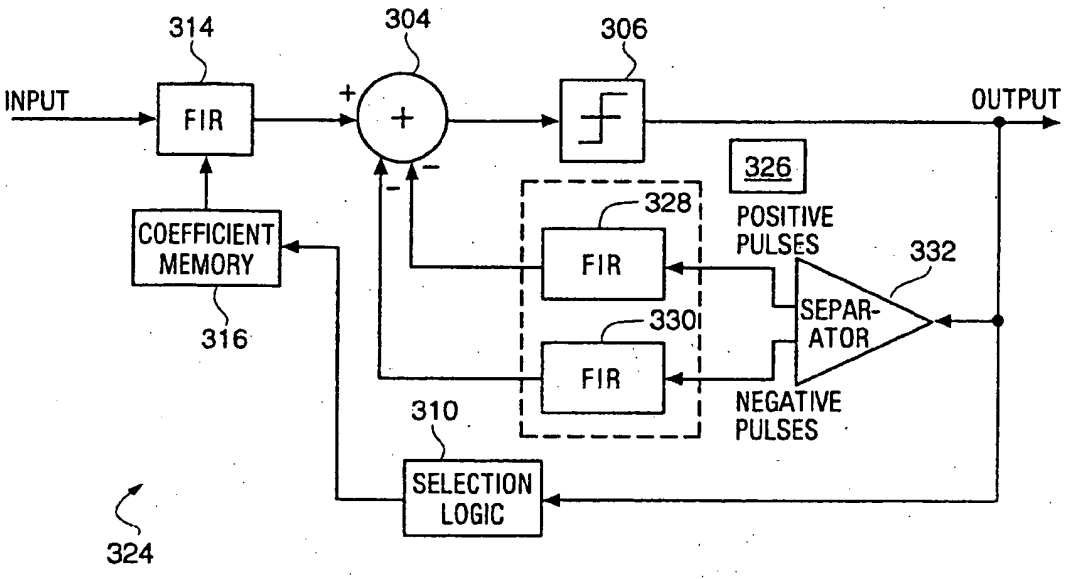
COEFFICIENT MEMORY
FIR
316
322
COEFFICIENT MEMORY
310
320
SELECTION LOGIC

FIG. 2C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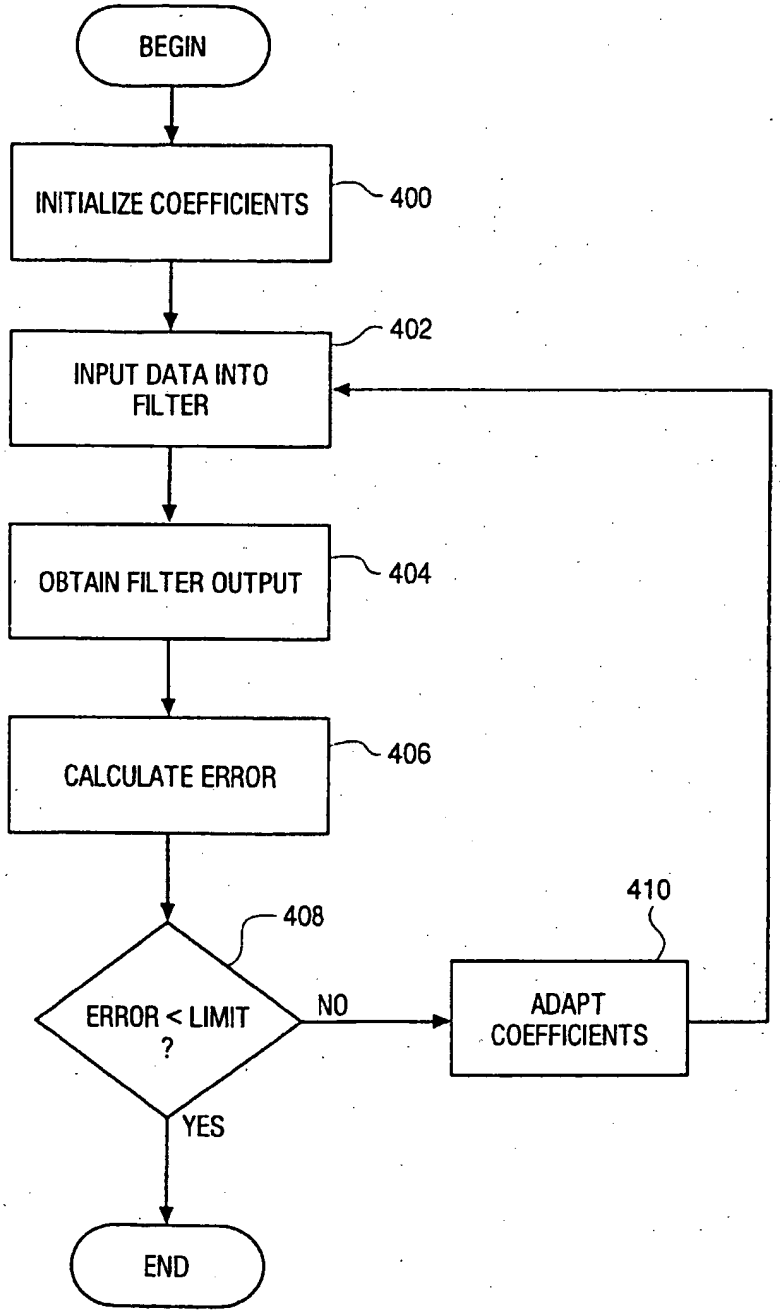
310
NEGATIVE
PULSES
SELECTION
LOGIC
324

FIG. 2D

FIG. 3


BEGIN
INITIALIZE COEFFICIENTS
400
INPUT DATA INTO FILTER
402
OBTAIN FILTER OUTPUT
404
CALCULATE ERROR
406
ERROR < LIMIT ?
408
NO
ADAPT COEFFICIENTS
410
YES
END

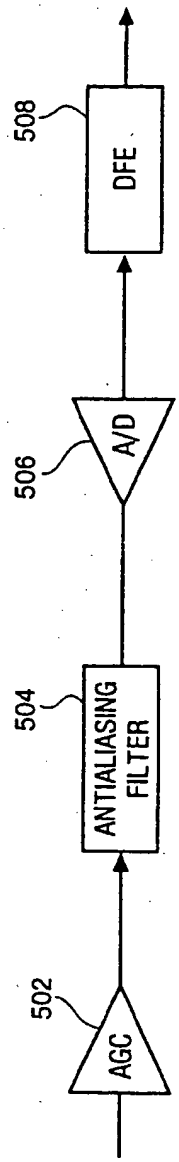


FIG. 4

FIG. 5A

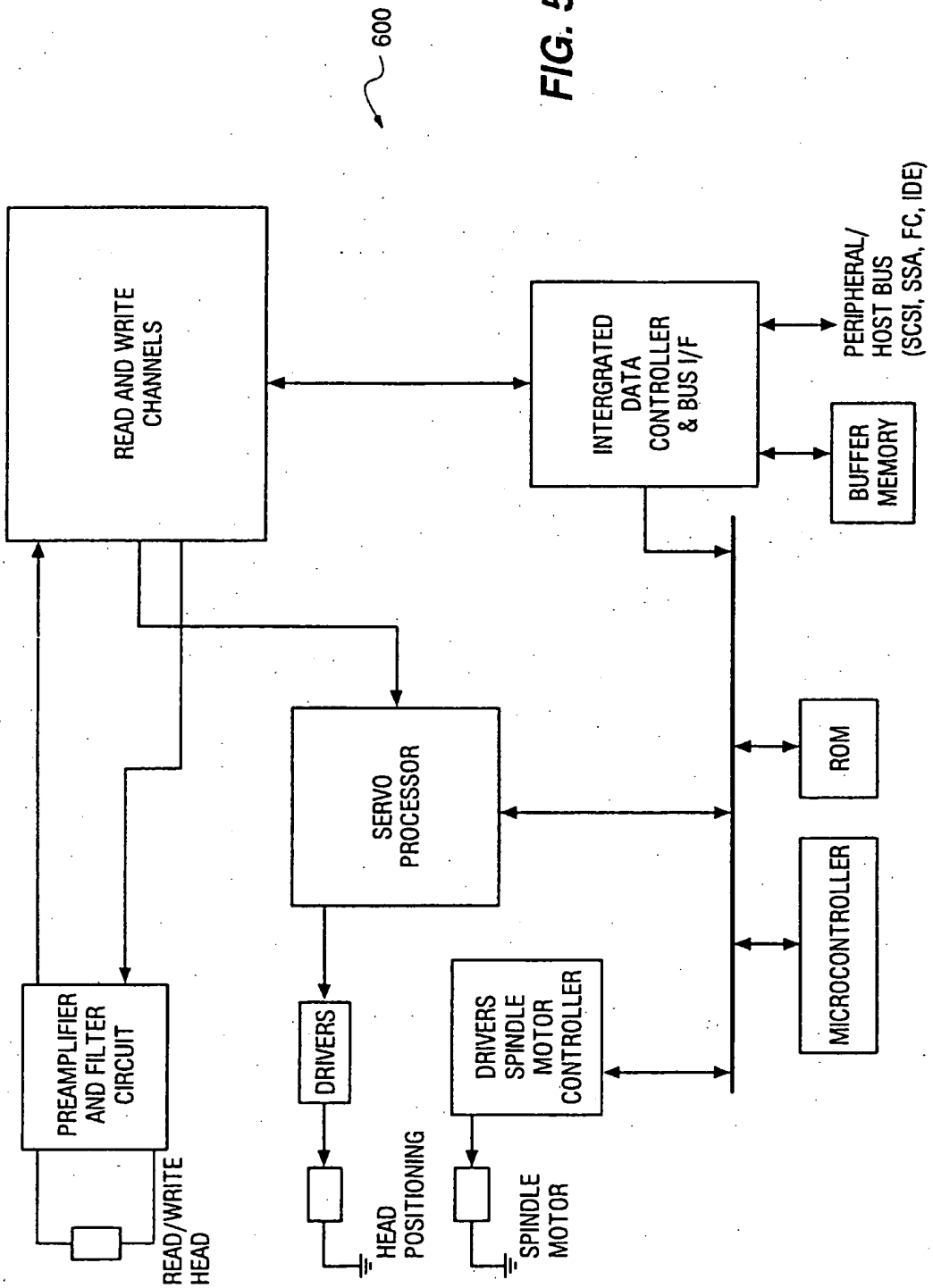
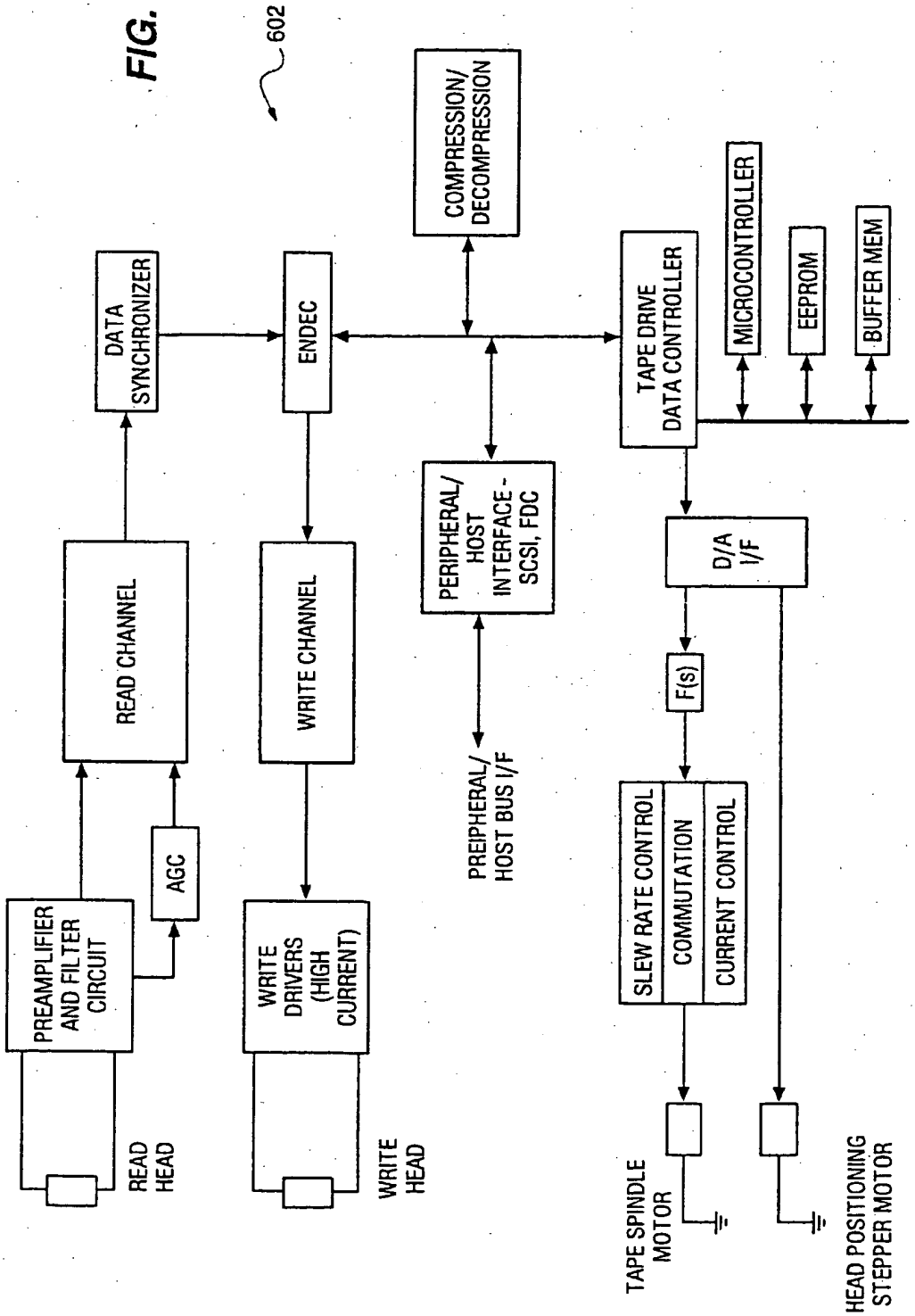

600
READ AND WRITE CHANNELS
INTERGRATED DATA CONTROLLER & BUS I/F
PERIPHERAL/ HOST BUS (SCSI, SSA, FC, IDE)
BUFFER MEMORY
SERVO PROCESSOR
ROM
MICROCONTROLLER
PREAMPLIFIER AND FILTER CIRCUIT
DRIVERS
DRIVERS SPINDLE MOTOR CONTROLLER
READ/WRITE HEAD
HEAD POSITIONING
SPINDLE MOTOR

FIG. 5B


602
COMPRESSION/ DECOMPRESSION
DATA SYNCHRONIZER
ENDEC
TAPE DRIVE DATA CONTROLLER
MICROCONTROLLER
EEPROM
BUFFER MEM
READ CHANNEL
WRITE CHANNEL
PERIPHERAL/ HOST INTERFACE - SCSI, FDC
D/A I/F
F(s)
PREAMPLIFIER AND FILTER CIRCUIT
AGC
WRITE DRIVERS (HIGH CURRENT)
PREIPHERAL/ HOST BUS I/F
SLEW RATE CONTROL
COMMUTATION
CURRENT CONTROL
READ HEAD
WRITE HEAD
TAPE SPINDLE MOTOR
HEAD POSITIONING STEPPER MOTOR

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(51) Int Cl.[6]: **H04L 25/03**, G11B 20/10

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(54) Digital signal processing apparatus and method

(57) The invention provides for signal processing apparatus (100) having a first filter means (102) for adjusting an input signal based on past data output from the apparatus (130), a summing means (106) is arranged to sum signals from the first filter means (102) and from a second filter means (104) to produce a sum signal. The apparatus also includes a symbol detection means (108) for generating an output signal from the sum signal and the second filter means (104) is arranged to provide adjustments in the output signal based on the peaks and polarity of past signals generated by the symbol detection means (108). A control means can be included for controlling the filtering properties of both the first and second filter means, wherein the control means controls the filtering properties based on the past output signals from the symbol detection means.

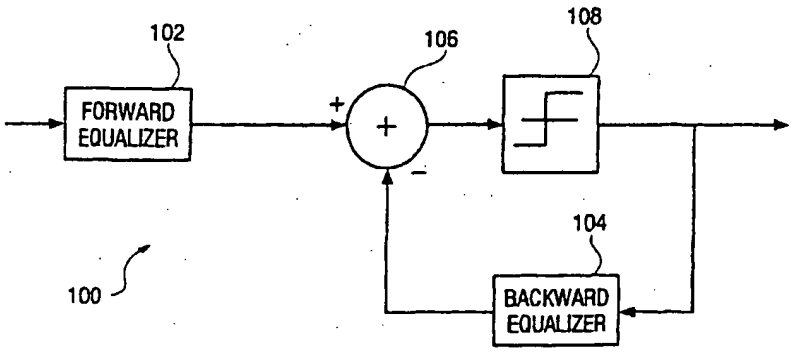

FIG. 1

EP 0 808 046 A3

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EUROPEAN SEARCH REPORT

Application Number
EP 97 30 3195

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
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A	US 5 471 504 A (LEE JUNGHSI ET AL) 28 November 1995 --- -/--		

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 May 1999	Schiwy-Rausch, G

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& : member of the same patent family, corresponding document

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EUROPEAN SEARCH REPORT

Application Number
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26-05-1999

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US 5471504 A	28-11-1995	NONE	

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82